



Enhancing 5G LTE Communications: A Novel LDPC Decoder for Next-Generation Systems



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Received: 12-27-2023

Revised: 02-10-2024

Accepted: 03-11-2024

Citation: D. Y. Venkatesh, K. Mallikarjunaiah, M. Srikantaswamy, and K. Huang, "Enhancing 5G LTE communications: A novel LDPC decoder for next-generation systems," *Inf. Dyn. Appl.*, vol. 3, no. 1, pp. 47–63, 2024. <https://doi.org/10.56578/ida030104>.



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Abstract: The advent of fifth-generation (5G) long-term evolution (LTE) technology represents a critical leap forward in telecommunications, enabling unprecedented high-speed data transfer essential for today's digital society. Despite the advantages, the transition introduces significant challenges, including elevated bit error rate (BER), diminished signal-to-noise ratio (SNR), and the risk of jitter, undermining network reliability and efficiency. In response, a novel low-density parity check (LDPC) decoder optimized for 5G LTE applications has been developed. This decoder is tailored to significantly reduce BER and improve SNR, thereby enhancing the performance and reliability of 5G communications networks. Its design accommodates advanced switching and parallel processing capabilities, crucial for handling complex data flows inherent in contemporary telecommunications systems. A distinctive feature of this decoder is its dynamic adaptability in adjusting message sizes and code rates, coupled with the augmentation of throughput via reconfigurable switching operations. These innovations allow for a versatile approach to optimizing 5G networks. Comparative analyses demonstrate the decoder's superior performance relative to the quasi-cyclic low-density check code (QCLDC) method, evidencing marked improvements in communication quality and system efficiency. The introduction of this LDPC decoder thus marks a significant contribution to the evolution of 5G networks, offering a robust solution to the pressing challenges faced by next-generation communication systems and establishing a new standard for high-speed wireless connectivity.

Keywords: Low-density parity check; Quasi-cyclic low-density check code; Bit error rate; Signal-to-noise ratio; 5G long-term evolution

1 Introduction

The method of delivering and receiving signals by channel is known as communication. Mistakes may occur within the acquired signal during the transportation of a signal from a source to a destination in a communication system due to a variety of impediments. As a result, in order to retrieve the original message, error repair is required. Robert Gallager invented LDPC codes in 1963. The researcher looked at the codes and discovered that LDPC codes effectively increased the Shannon capacity of an energy harvesting transmitter communicating over additive white Gaussian noise (AWGN) and binary erasure channels [1]. Transmission mistakes can be repaired using error-correcting codes and clever mathematical procedures. Channel coding is the term for this. Codes can also be used to reduce the number of bits required to provide legitimate data, a process known as source coding [2, 3]. This study deals with channel coding schemes for two critical communication systems, which shows that, by employing effective channel coding schemes in these systems, their overall performance may be improved in a variety of ways, bringing them to practical applications in the real world [4–6]. In the literature, authors have proposed a hybrid decoding algorithm by applying linear approximation with non-linear functions to the Belief Propagation (BP) algorithm, as shown in Figure 1.

The main aim of the present research work is to develop a high-performance and area-efficient 5G LDPC decoder. In the conventional method to construct the 5G LDPC codes, a low-density generator matrix (LDGM) code and

a high-rate LDPC code are concatenated [7, 8]. The variable nodes (VNs) in LDGM are 1-degree VNs, which receive the message from one check-to-variable (CTV) in each iteration and are reliable for the CTV messages received. Therefore, a fixed point with low quantization and a limited correction component was implemented. The degradation of overall performance is effected by the Optimized Min-Sum (OMS) decoder [9]. In recent years, several algorithms have been proposed to improve the performance of error correction for 5G LDPC codes. In much research work, generalized approximate-min algorithms are proposed by considering the approximate-min algorithm. Due to the implementation complexity, they suffer enormously, just like the BP decoding with concerned non-linear capabilities.

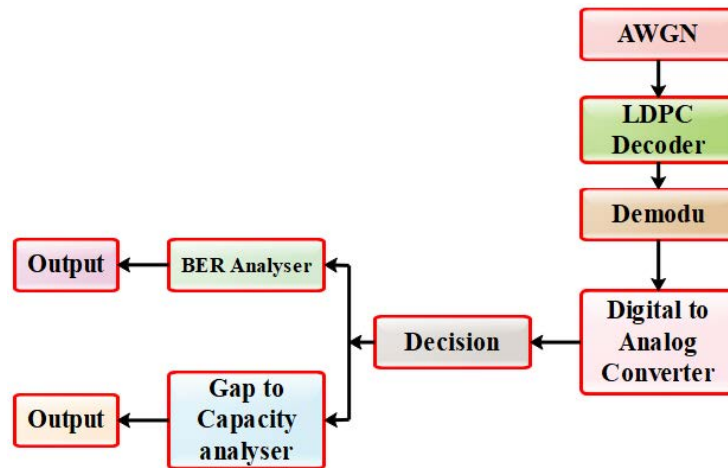


Figure 1. Block diagram for decoding

1.1 Background on 5G LTE

In modern communication systems, particularly in the context of 5G LTE technology, the significance of error-correcting codes cannot be overstated. 5G LTE represents a leap forward in telecommunications, offering vastly improved data rates, reduced latency, and increased connectivity for a myriad of devices. However, the very features that empower 5G LTE, such as higher frequency bands and dense network environments, also make it more susceptible to various types of transmission errors. These errors can stem from factors like signal fading due to longer distances or obstacles, interference from the increased number of devices and base stations, and the inherent vulnerabilities of moving at high speeds, which are especially relevant for mobile communications [10]. Error-correcting codes are integral to mitigating these challenges. They enhance the reliability of data transmission across the 5G network by identifying and correcting errors that occur during signal transmission. This is critical to maintaining the high-speed, high-quality communication expected of 5G LTE. The types of errors that can impact 5G LTE include bit errors, where individual bits are flipped from 0 to 1 or vice versa; burst errors, which affect a string of consecutive bits; and packet errors, where entire blocks of data are lost or corrupted. These errors can degrade the quality of service, causing video streams to buffer, voice calls to drop, and critical data transmissions to fail [11]. Error-correcting codes in 5G LTE, such as Turbo codes, LDPC codes, and Polar codes, are designed to address these issues efficiently. They enable the system to detect and correct errors without needing to retransmit data, thus saving bandwidth and reducing latency. This is particularly important for applications requiring real-time communication, such as autonomous driving, remote surgery, and interactive virtual reality, where even minimal delays or data inaccuracies could lead to significant consequences. By ensuring data integrity and reliability, error-correcting codes play a pivotal role in fulfilling the promise of 5G LTE as a cornerstone of modern digital infrastructure [12].

1.2 Research Gap

Despite the rapid advancements in 5G LTE technologies, a critical challenge persists in the form of signal errors that compromise data transmission reliability and efficiency. Current literature offers extensive insights into error correction methods, yet there's a notable gap in the targeted evaluation of these methods within the 5G LTE framework. The unique challenges posed by 5G LTE, such as higher susceptibility to interference, signal fading, and the demands of supporting high data rates with minimal latency, necessitate a nuanced approach to error correction. This gap underscores the need for an in-depth investigation into the types of errors that predominantly affect 5G LTE and the effectiveness of existing error-correcting codes in this specific context [13–15].

1.3 Aim and Contribution

This research aims to bridge this research gap by conducting a comprehensive analysis of error types in 5G LTE and assessing the performance of current error-correcting codes against these challenges. The objectives are threefold: firstly, to catalog and analyze the prevalent errors in 5G LTE systems; secondly, to evaluate the efficacy of existing error correction strategies within this context; and thirdly, to propose refinements or new error-correcting approaches tailored to enhance 5G LTE reliability and efficiency. By addressing these aims, the proposed work contributes significantly to the telecommunications field. It not only deepens the understanding of error correction needs in 5G LTE but also introduces practical solutions that could pave the way for more robust and efficient 5G communication systems. Through this focused approach, the paper endeavors to fill the identified research gap, thereby facilitating improvements in 5G LTE technology that are essential for its broader adoption and success in various applications [16].

1.4 Hybrid Decoding Algorithm

The hybrid decoding algorithm emerges as a pivotal innovation in the landscape of 5G communication, specifically designed to enhance the performance of LDPC decoders. This algorithm ingeniously synthesizes the strengths of two well-established decoding techniques, namely, the BP and the Min-Sum (MS) algorithms, to address the twin imperatives of decoding efficacy and computational efficiency that are critical for the next generation of wireless networks [17].

At its core, the BP algorithm is celebrated for its exceptional error-correcting performance, utilizing probabilistic message passing to accurately predict and correct bit errors within transmitted data. However, this accuracy comes at a cost, necessitating substantial computational resources and power, which can be a limiting factor in resource-constrained environments typical of mobile and embedded systems. Conversely, the MS algorithm offers a streamlined alternative that, while slightly less precise in error correction, significantly reduces the computational burden and hardware footprint, making it an attractive option for systems where efficiency is paramount [18].

The hybrid decoding algorithm operates by dynamically assessing the error landscape of each LDPC code block received, leveraging real-time analysis to determine the most appropriate decoding strategy. For code segments where the error probability is high or in scenarios demanding the utmost in reliability, such as critical communications infrastructure or high-speed mobile connections, the algorithm opts for the BP approach to maximize error correction. In contrast, for segments with lower error probabilities or when optimizing for power and hardware efficiency, it switches to the MS algorithm. This dual-strategy approach allows the algorithm to adaptively optimize its decoding process, ensuring that it maintains a high level of decoding accuracy without unduly taxing the system's computational and hardware resources [19].

The significance of the hybrid decoding algorithm within the 5G LDPC decoding context cannot be overstated. By harmonizing the error-correcting power of the BP algorithm with the computational elegance of the MS algorithm, it addresses one of the most pressing challenges in 5G communication: how to achieve ultra-reliable, high-speed data transmission in an environment that is inherently resource-constrained and variable. This algorithm not only enhances the robustness and efficiency of 5G LDPC decoders but also contributes to the broader goal of making 5G technology a viable, scalable solution for an array of applications, ranging from Internet of Things (IoT) deployments to ultra-reliable, low-latency communications and beyond. In doing so, the hybrid decoding algorithm stands as a testament to the ongoing evolution of communication technology, driving forward the capabilities of 5G networks to meet the demands of the digital age [20].

Recent advancements in 5G LDPC code enhancement have introduced notable algorithms like the Layered BP (LBP) and OMS algorithms. The LBP algorithm accelerates error correction by processing codes in layers, leading to faster convergence and improved throughput, although it may falter in highly noisy conditions. On the other hand, the OMS algorithm refines error correction with dynamically adjusted scaling factors for a better balance between performance and complexity, requiring precise tuning under varying network conditions. Both algorithms aim to boost the reliability and efficiency of 5G communications, each with unique strengths and limitations that contribute to the evolving landscape of 5G technology.

1.5 QCLDC

The QCLDC method serves as a benchmark for evaluating the performance of a newly proposed LDPC decoder optimized for 5G LTE communications. The abstract outlines a scenario where the advent of 5G technology, despite offering high-speed communication capabilities, introduces challenges such as increased BER, reduced SNR, and the potential for jitter. These issues necessitate advanced error-correcting mechanisms to ensure reliable data transmission [21].

The proposed LDPC decoder is presented as a solution specifically designed to address these challenges within 5G networks. It aims to lower the BER, improve the SNR, and enhance both switching and parallel operations, crucial for the efficient handling of the massive data flows characteristic of 5G technology. The decoder's capability

to dynamically adjust message size and code rate, along with its improved throughput via reconfigurable switching operations, signifies a significant advancement over traditional methods, such as the QCLDC.

By comparing the performance of this new LDPC decoder against the QCLDC method, the abstract highlights the former's superior performance through simulation results. This comparison underscores the innovative decoder's effectiveness in enhancing communication quality and system efficiency within 5G networks. The advancements outlined suggest that the LDPC decoder not only addresses the immediate challenges posed by 5G technology but also sets a new benchmark for future developments in wireless communication systems, offering a more reliable and efficient solution for managing the complexities of next-generation networks.

2 Relative Work

A comprehensive survey on the LDPC decoder for 5G LTE technology has been carried out in order to carry out the work that has been recommended. This survey was based on the challenges of deterioration in noisy environments, balancing error correction and efficiency, SNR, and other factors. A comparison of the work that has been done in the field of LDPC is presented in Table 1.

3 Methodology

LDPC codes are widely used in modern communication systems, including 5G LTE, due to their excellent error-correcting capabilities. Designing an LDPC decoder for a next-generation communication system like 5G LTE requires a well-structured methodology. This section presents a high-level outline of the methodology for developing an LDPC decoder with the 5G LTE algorithm.

3.1 Shannon Channel Coding Theorem

The Shannon channel coding theorem in information theory is understood to have endorsed the development of error control codes [17–19]. It states that all the data rates much less than the channel capacity may be done with an arbitrarily small chance of error, which is given by the Shannon-Hartley Eq. (1).

$$C = T_p * \log_2 \left(1 + \frac{S_p}{N_p T_p} \right) \quad (1)$$

where, C is the channel capacity, T_p represents the transmission bandwidth, S_p is the signal power, and N_p is the spectral density of noise power [20].

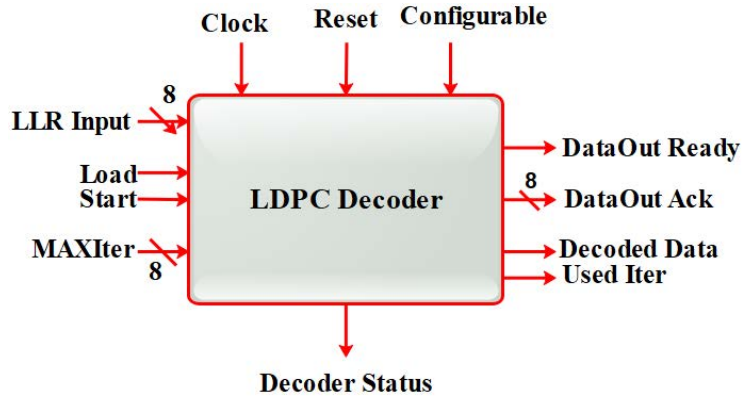


Figure 2. Block diagram of the designed LDPC decoder

Figure 2 shows the block diagram of the designed LDPC decoder, which consists of synchronous reset inputs and a global clock. Based on the provided value at the MaxIter input, the iteration's permissible range is decided between 0 and 15. The value of MaxIter is read by setting the "configure" to high. Through the control signal of the load, the log-likelihood ratios (LLRs) are fed into the decoder. The start signal is used to initiate the decoding process. After the completion of the decoding process, the decoded data is collected through the signal "data out ready." For the confirmation of data receipt, the decoded bit "Data Out Ack" is used. The "used Iter" port is used to acquire the iteration range. The progress of the decoder is shown by the port "decoder status," which shows the active and idle states.

Table 1. Comparison of studies in LDPC

No.	Title	Authors	Technology	Drawbacks	Year
1	[22]	F. Li et al.	5G LDPC codes	High computational complexity	2021
2	[23]	K. J. Sampath et al.	Layered BP	Performance degradation in noisy environments	2014
3	[24]	J. Shrinidhi et al.	Optimized MS	Demand for precise scaling factor tuning	2020
4	[25]	A. Muskan et al.	Hybrid algorithms	Balance between error correction and efficiency	2023
5	[26]	Ankita Pramanik et al.	5G LDPC codes	Susceptibility to error floors	2018
6	[27]	V. L. Petrović	Focus on achieving high data processing speeds	Possible increase in error rates in scenarios with low SNR	2022
7	[28]	K.-H. Lin et al.	Design of codes that scale efficiently across networks	Complexity challenges in large-scale deployments	2011
8	[29]	A. Jemima and G. Manoj	Reduction of decoding time to meet 5G's low-latency requirements	Potential compromises on decoding accuracy for speed	2023
9	[30]	L. Chen et al.	Optimization of power consumption for IoT devices	Possible consequences of lower decoding performance to save energy	2020
10	[31]	H. Li et al.	Enhancement of resilience against a wide range of errors	Complex implementation and optimization	2005
11	[32]	Y. Wang and S. Che	Adaptation of decoding strategies dynamically	Introduction of overhead from dynamic adaptation mechanisms	2024
12	[33]	M. Zhang et al.	Aim for superior processing speeds in communication	Synchronization challenges in high-speed contexts	2024
13	[34]	M. Zhang et al.	Adaptation of LDPC codes for 5G New Radio (NR) specifics	Demand for sophisticated design efforts and custom hardware	2024
14	[35]	P. S. Wulandari et al.	Preparations for future quantum computing threats	Challenges in decoding time and complexity	2023
15	[36]	M. Elkadi et al.	Utilization of artificial intelligence (AI) to refine LDPC code performance	Heavy dependence on extensive datasets for effective training	2021
16	[37]	Y. Lyu et al.	Implementation of LDPC decoders on the Field-Programmable Gate Array (FPGA) for flexibility and speed	Possible limitations in scalability and higher power consumption	2023

The LLR input is loaded one after another serially to the decoder, and the decoded data is also latched serially bit by bit through the “decoded data” port. This process of decoding is used because of the FPGA input/ output ports available [38–40].

3.2 Top-Level Architecture

The quantization version is predicted using LLR messages and decoded in the input port. Quantization and LLR messages are important components in the context of LDPC decoding. The LLR messages represent the likelihood of bits being either 0 or 1, and quantization is a process of mapping these continuous LLR values to discrete symbols (0 or 1) for further processing. This is commonly done in LDPC decoding to facilitate the message-passing algorithm,

such as BP. The CTV messages compressed are shown in Figure 3.

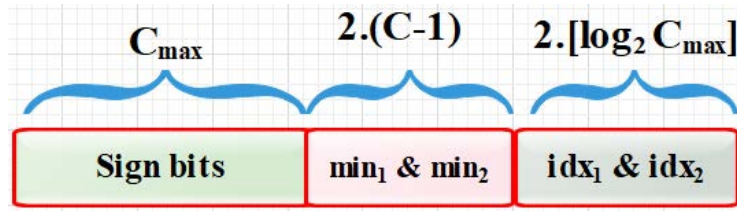


Figure 3. Compressed format of CTV messages

The base matrix HB , corresponding to a QC-LDPC with dimensions $Mb \times Nb$ and a decoding layer range L , is observed to typically equal Mb . This equality suggests that the expansion factor Z directly correlates with the parallelism degree of the decoder. It is noted that the values of a posteriori probability (APP) q-bits are subjected to quantization, ensuring that the messages exchanged are represented with q-bit precision. All control signals are generated. All control signals are generated by the controller. The CTV and APP messages are stored in blocks of two memories, CTV memory and APP memory, respectively. The dual-port random access memory (DP-RAM) aids simultaneous write and read operations. The operations of read, write, and begin are performed in parallel with the APP memory, which uses registers. The memory of APP is classified into three portions in the suggested architecture, and the memory of CTV is divided into two parts [41–43].

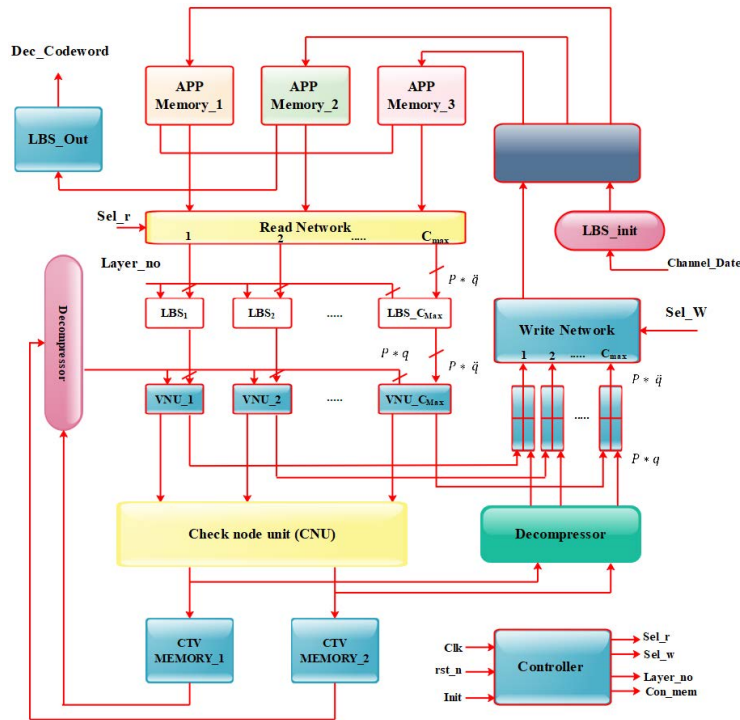


Figure 4. Top-level architecture of the proposed 5G LTE-based LDPC decoder

Figure 4 shows the top-level architecture of the proposed 5G LTE-based LDPC decoder. During the decoding process, the APP messages are taken from APP memory, and then they forward into the read network, where they rearrange to choose the message for the processing layer in accordance with the VN units (VNUs) and left barrel shifters (LBSs). In the same manner, APP messages are organized to update the write network; hence, they can be stored in the APP memory addresses [44, 45]. The code of the maximum is represented by C^{\max} of VNUs and LBSs adopted in the proposed architecture. The read network message is turned left through LBSs in line with the shift factors to calculate VTC messages. The barrel shifter data write-back may be avoided by using the approach given to produce the shift factor [46–48].

CNU's architecture is separated into subunits, as seen in Figure 5. The VTC message units are applied to the 1st CNU and the 2nd CNU, respectively, when orthogonal layers are processed simultaneously. The Compare and Select units are deactivated in this scenario, so CTV message units are output from the CNU. In the orthogonal section, let c be the greatest row degree. The width of CTV memory is set to 512 bytes in order to store sets of CTV messages

at the same address, and the CTV memory process has been done using Eq. (2).

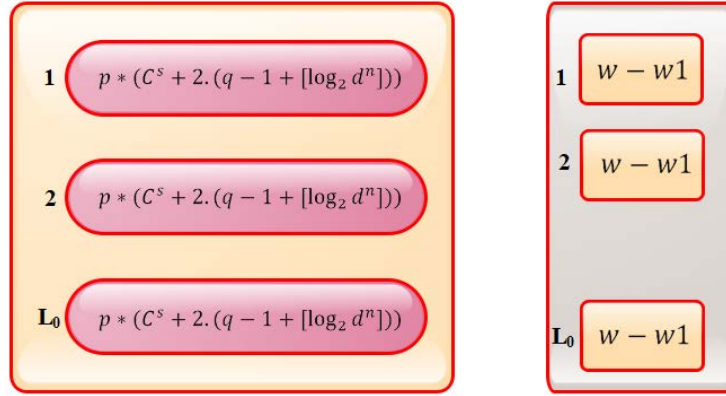


Figure 5. Architecture of the CNU

$$w = \max \{p * (c^{\max} + 2 * (q - 1 + j \log_2 c^{\max})), 2 * p * (c^d + 2 * (q - 1 + s \log_2 c^d))\} \quad (2)$$

The memories of CTV are divided into parts. The orthogonal components, and the maximum row degree of layers except the core, $W_1 = p (n_d c + 2 (q - 1 + \log_2 n_d c))$ denote the detailed structure of those submemories. The initial segments W_1 of CTV messages are generated within the core. Orthogonal components are stored in CTV memory 1, and the rest are stored in memory 2 of CTV, as shown in Figure 6.

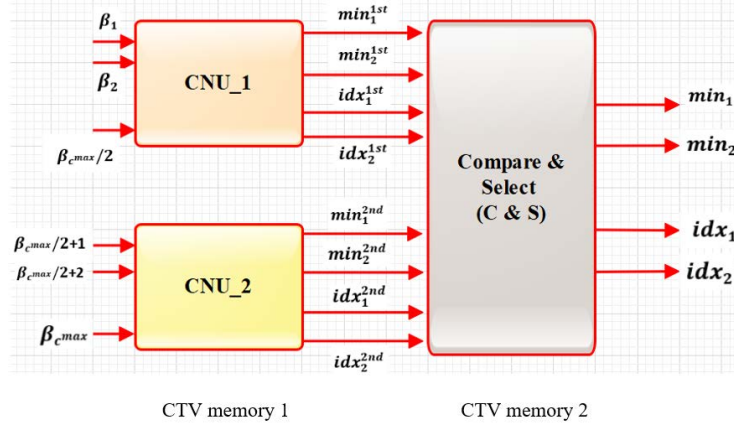


Figure 6. Detailed structure of the CTV memory

The messages of CTV are absolutely saved in memory CTV 1 for distinct levels. CTV memory 2's depth $L0$ is substantially shorter than L since it is only used for the layers in the centre and orthogonal regions. In addition, the scale of memory CTV is reduced by 16.6% for codes BFI and by 18.4% for codes BG2. In sum, of CTV RAM, 39.6% is saved for BG1, and 29.8% of BG2 is used in the layer merging method. Because the CTV memory consumes such a large portion of the decoder's area, these solutions have a considerable impact on overall area reduction. The interconnection block, which determines the overall hardware overhead, is another important component of the memory block [49–53].

During the decoding process, the APP messages are taken from APP memory. Then it forwards into the read network, and rearranges to choose the message for the processing layer in accordance with the VNUs and LBSs. In the same manner, APP messages are organized to update the write network; hence, they can be stored in the APP memory addresses as shown in Figure 7.

This algorithm, which is also employed in the AI field, is found in Gallagher's work. It is characterized by the probabilistic model governing the transmission of messages from a message node c to check nodes. This model takes into account the value v observed at the node as well as the value communicated to v in the preceding round. The transfer of messages from c to v is likely to have certain values from the last round. Under a particular assumption known as the assumption of independence, it is simple to construct formulas for these probabilities [54, 55].

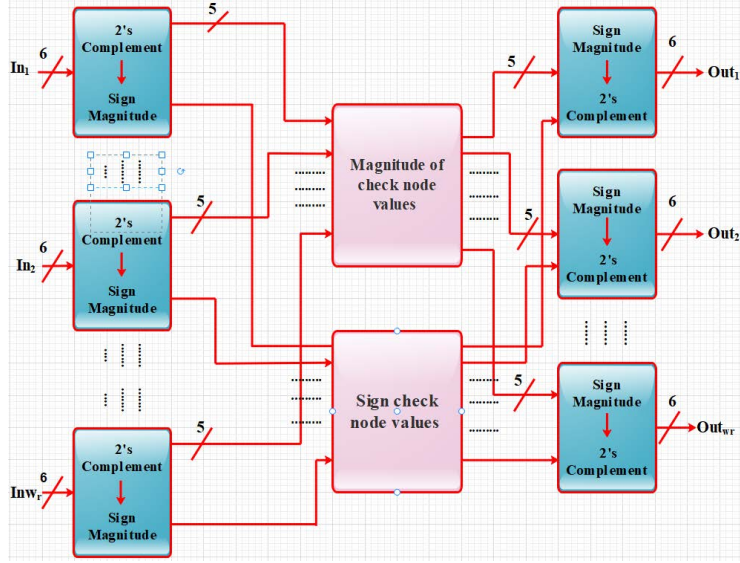


Figure 7. APP memory for the structure of extension bits

Working with log-likelihoods and likelihoods rather than probabilities is occasionally helpful. The likelihood probability is given in Eq. (3), which articulates the formulation of the likelihood probability x for a binary random variable.

$$\text{Let } L(X) = P_r[x = 0] / P_r[x = 1] \quad (3)$$

By Baye's rule, if x is an equiprobable random variable, then $L\left(\frac{x}{y}\right) = L\left(\frac{y}{x}\right)$.

As a result, if $[y_1, y_2, y_3, y_4 \dots \dots y_d]$ are random variables that are independent of one another, as shown in Eqs. (4) and (5), then:

$$\ln L(x | y_1, \dots y_d) = \sum_{i=1}^d \ln L(x | y_i) \quad (4)$$

$$\ln L(x_1 \oplus \dots \oplus x_l | y_1 \dots \dots y_l) = \ln \frac{1 + \left(\prod_{i=1}^l \tanh\left(\frac{l_i}{2}\right)\right)}{1 - \left(\prod_{i=1}^l \tanh\left(\frac{l_i}{2}\right)\right)} \quad (5)$$

where, I is equal to $\ln x_i / y_i$.

3.3 Check Node Processing

In LDPC decoding, check node processing is a crucial step in the BP, or sum-product algorithm (SPA), used to correct errors in received data. Check node processing occurs in the second phase of the BP algorithm and is responsible for updating the information about parity checks in the LDPC code. The check node values are computed using the second step of the logarithmic message. The check node values are computed using the second step of the logarithmic message forwarding technique. As seen below, the check node values $L(r_{ji})$ are generated from the VN values L_{qij} . Check node processing has been conducted using Eq. (6). Figure 8 represents the output generation of its input by adding all W_r inputs to the output of check nodes.

$$L(r_{ji}) = \prod_{i \in R_{ii}} \alpha_{ij} \cdot \emptyset \left(\sum_{i \in R_{ii}} \oint (\beta_{ij}) \right) \quad (6)$$

where, $\alpha_{ij} = \text{sign}(L(q_s))$, $\beta_q = |L(q_{ij})|$, and $\emptyset(z) = \log \frac{e^z + 1}{e^z - 1}$.

The magnitude of the check nodes is computed according to Eq. (7).

$$|L(r_{ji})| = \varphi \left(\sum_{i \in R_{ji}} \varphi(\beta_{ij}) \right) \quad (7)$$

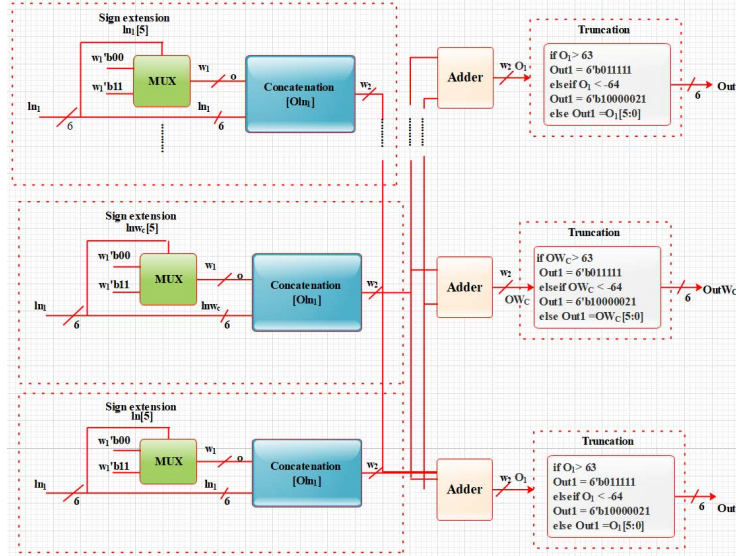


Figure 8. Check node values for magnitude computation

The LDPC decoding process starts with the initialization of VNs and check nodes. VNs represent bits, and check nodes represent parity checks in the LDPC code. The received LLRs are associated with VNs. Message passing uses the BP algorithm, and it occurs iteratively between VNs and check nodes. VNs send messages to connected check nodes, and check nodes send messages back to VNs [56–58].

3.4 Check Node Processing

During the check node processing step, check nodes calculate and send updated messages to VNs.

The message sent from a check node to a VN contains information about the parity constraints associated with that check node. The check node checks whether the parity constraints are satisfied based on the LLRs received from the connected VNs.

The messages typically represent soft information and are updated using the SPA. The SPA involves the following steps:

- Message calculation: The check node calculates a message for each connected VN by summing or combining the LLRs from the connected VNs.

- Message update: The calculated messages are sent to the respective VNs. These messages can be thought of as “soft constraints” based on the parity checks.

3.5 Flow Chart

Binary Phase Shift Keying (BPSK) modulation is used in this example, which transforms a code in sequence $C = C_1, C_2, \dots, C_n$. Then S is sent over an AWGN channel. Following demodulation, the obtained value for S_i is $Y_i = S_i + n_i$. Then $L(P_i)$ is calculated from the received value Y_i . Bit i is transferred from check node j to VN I . Then the LLR $L(q_{ij})$ of bit i is transferred from VN I to check node j . At each iteration, $L(Q_i)$ is the posteriori LLR of bit i .

The flow chart of the BP decoding algorithm is shown in Figure 9.

$$L(r_{ji}) = (\pi c > i'j) \dots \dots, E \sim n) (t J i'j) \quad (8)$$

For ease of reference in subsequent discussions, the following notations are introduced:

$R(j)i$: Check node j connected by all VNs, excluding VN i .

$C(i)j$: VN i associated with all check nodes excluding check node j .

$L(P_i)$: The LLR.

$L(r_{ji})$: Bit i of VN_i is transferred from check node j and the LLR of bit i .
 $L(q_{ij})$: The LLR of bit i is moved from VN_i to check node j .
 $L(Q_i)$: The posteriori LLR of bit i .

The BP decoding technique is depicted in Figure 9 as a flow chart. The process goes back to step 1 if the number of repetitions is the maximum and if it is not a valid code word [59–63]. The BP algorithm works well for codes such as LDPC, but the tanh and tanh-1 operations are too difficult to implement in hardware. Otherwise, the minsum technique makes updating messages in check nodes faster to calculate by using a clever approximation of the conventional BP algorithm, as given in Eq. (9).

$$L(r_{ji}) = \left(\prod_{i' \in R(j) \setminus i} \emptyset_{i'j} \right) (\min(\beta_{i'j})) \quad (9)$$

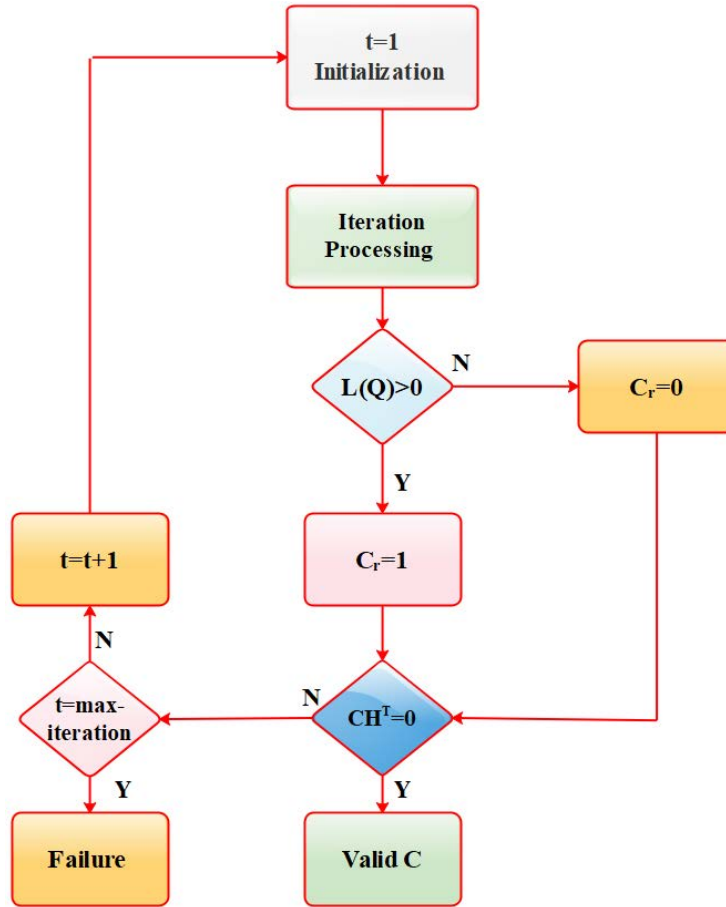


Figure 9. Flow chart of the BP algorithm

The computed values for a particular pair of I, j are denoted by L_1, L_2 , which have the same sign, and $IL_2 > IL_1$. The performance is approximated based on the offset BP-based algorithm while containing only adds and comparisons, making it appropriate for hardware implementation [64]. To compensate for the min-sum hardware implementation [64]. To compensate for the min-sum approximation's performance loss, it was calculated using Eq. (10).

$$L(r_{ji}) = \left(\prod_{i' \in R(j) \setminus i} \emptyset_{i'j} \right) \cdot \max(\min(\beta_{i'j}) - \rho, 0) \quad (10)$$

3.6 Decoder for an AWGN Channel

For an LDPC code, a tanner graph is a bipartite graph in which one class of nodes corresponds to n bits in the code word and the other class corresponds to VNs. The second sort of node is the check node, which corresponds

to m parity check equations. An edge connects a VN to the check node if and only if that particular bit is included in the parity check equation [65]. The bit nodes in the Tanner graph are known as repetition nodes, whereas the check nodes are known as zero-sum nodes. The incoming data at each bit node corresponds to a single variable only, similar to how a repetition code works. The parity check constraint, often known as the zero-sum constraint, relates to the incoming data at each check node [66]. As a result, the belief propagation decoder is divided into two parts: a Soft Input Soft Output (SISO) decoder for a repetition code and a SISO decoder for a Single Parity Check (SPC) code. The i -th zero-sum node is represented in Eq. (11), where the i -th repetition node $m_i = r_i \times \sum_{j=1}^{w_c-1} L_i$.

$$L_i = S_i \times \sum_{j=1}^{w_r-1} |\log(\tanh |m_i/2|)| \quad (11)$$

4 Results and Discussion

In this section, the performance analysis has been done between the proposed algorithm and conventional methods with an $N_b=672$ block code. Figure 10 shows the performance analysis between the proposed method and conventional methods for $R=1/2$. Figure 11 shows the performance analysis between the proposed method and conventional methods for $R=13/16$. Figure 12 shows the SNR performance analysis between the proposed method and conventional methods for $R=9/10$.

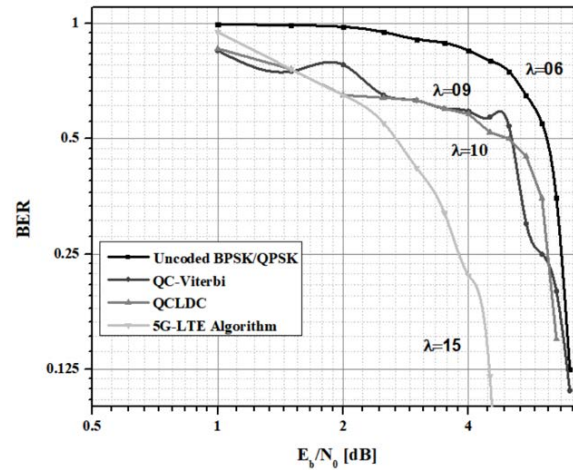


Figure 10. Performance analysis between the proposed method and conventional methods with respect to the code rate of 1/2

This analysis is predicated upon the variable $\frac{E_b}{N_0}$, representing the energy per bit to noise power spectral density ratio, articulated in decibels (dB). The delineation of BER performance as a function showcases the efficacy of the proposed method in contrast to conventional methodologies. The BER is plotted on a logarithmic scale which is common for such analyses, allowing for a wide range of error rates to be displayed clearly. Figure 11 shows the $\frac{E_b}{N_0}$ ratio on the x-axis, which represents the quality of the communication channel, with higher values indicating better channel conditions (less noise). The BER on the y-axis measures the rate at which errors occur in the received data stream. The lower the BER for a given $\frac{E_b}{N_0}$, the better the performance of the decoding algorithm.

Figure 11 shows the BER performance of various decoding schemes, including a proposed 5G-LTE algorithm, which is plotted against the $\frac{E_b}{N_0}$ ratio in dB. The uncoded BPSK/Quadrature Phase Shift Keying (QPSK) curve serves as the baseline, showing error rates without correction. The Quadrature Convolutional-Viterbi (QC-Viterbi) and QCLDC curves represent traditional and LDPC codes, respectively, both of which are standard in communications for error correction. Notably, the 5G-LTE algorithm's curve is expected to demonstrate enhanced performance, characterized by a lower BER across the $\frac{E_b}{N_0}$ spectrum, indicating superior error-correcting capabilities tailored for the 5G environment. Analyzing this graph involves assessing how each curve descends with increasing $\frac{E_b}{N_0}$, as a steeper descent indicates more effective error correction.

The proposed 5G-LTE algorithm's performance is of particular interest; if it maintains lower BER values at higher $\frac{E_b}{N_0}$ levels compared to the QC-Viterbi and QCLDC methods, it suggests a significant improvement in maintaining data integrity under typical 5G network conditions. This comparative analysis underscores the potential of the proposed algorithm to enhance the reliability of 5G communications, a key factor in supporting the network's high-speed and low-latency objectives.

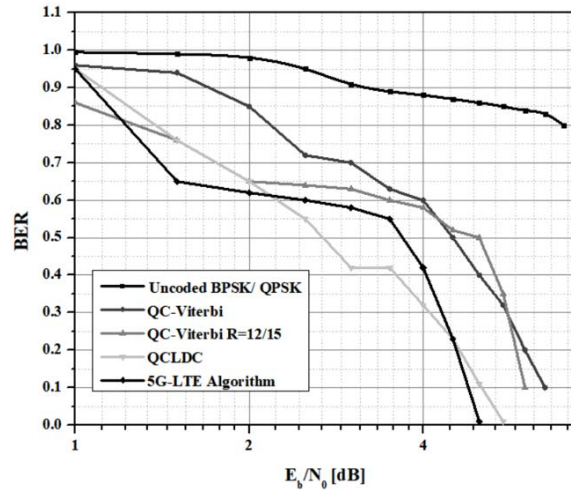


Figure 11. Performance analysis between the proposed method and conventional methods with respect to the code rate of 13/16

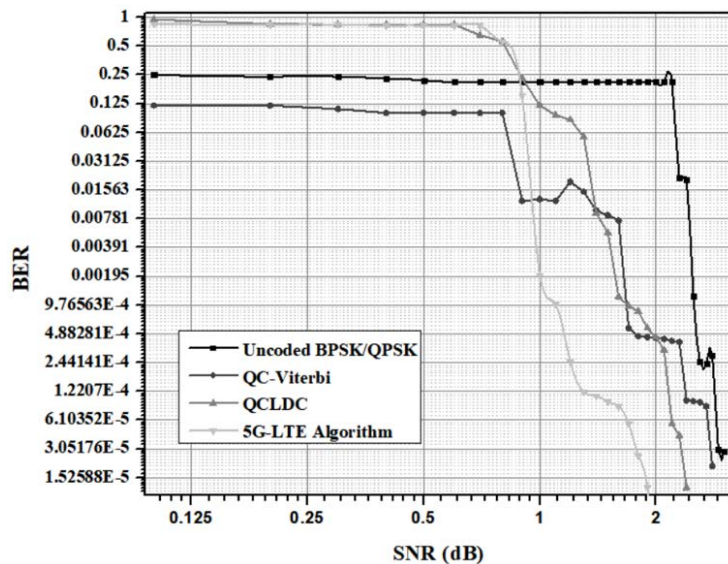


Figure 12. SNR performance analysis between the proposed method and conventional methods for R=9/10

Figure 12 shows the BER performance of several decoding schemes plotted against SNR in dB, which is a standard way to evaluate the efficacy of error correction in communication systems. The uncoded BPSK/QPSK curve establishes a baseline by showing the error rate without error correction, while the QC-Viterbi and QCLDC curves represent the performance of quasi-cyclic and LDPC codes, respectively. The 5G-LTE algorithm curve is included to illustrate the performance of the proposed method tailored for 5G networks. The steepness of the curve for the 5G-LTE algorithm, as compared to the QC-Viterbi and QCLDC, and its position relative to the uncoded BPSK/QPSK baseline, provide insight into its error-correcting performance. If the 5G-LTE algorithm's curve falls below the other curves at the same SNR levels, this would indicate a lower BER, signifying that the algorithm is more robust in correcting errors over the communication channel, especially in the noisy environments typical of 5G networks.

The 5G-LTE algorithm performs across different SNR values, particularly focusing on the lower end of the SNR spectrum, which is challenging for error correction algorithms. Superior performance at lower SNR values would mean that the 5G-LTE algorithm can maintain data integrity even in poor signal conditions, which is critical for the reliability of 5G communications. Additionally, the graph would be scrutinized for the SNR value at which each algorithm begins to flatten out, indicating the point at which further increases in SNR provide diminishing returns in error correction. This analysis would be crucial for understanding the practical applications and limitations of the 5G-LTE algorithm in real-world scenarios.

5 Conclusions

This study makes a significant contribution to the field of wireless communication by proposing a technique that enhances switching operations, facilitating the simultaneous control of multiple devices within a 5G communication infrastructure. The technique's ability to manage 64-bit operations with improved efficiency underlines its potential to handle complex tasks that are likely to be commonplace in the emerging IoT ecosystem.

The simulation results underscore the method's efficacy, demonstrating a notable reduction in the BER, namely, 2.5% over uncoded BPSK/QPSK, 1.6% over QC-Viterbi, and 0.5% over QCLDPC for a code rate (r) of 1/2. These improvements in BER directly translate to more reliable communication, with fewer errors and corrections needed, which is particularly valuable in applications requiring high data integrity. Moreover, the proposed method's enhancement of the SNR by 3.6%, 2.5%, and 1.3%, respectively, for the same methods and code rate further attests to its superior performance, offering clearer signal transmission and better overall network efficiency. For the higher code rate of 13/16, the BER improvements are 2.2% over uncoded BPSK/QPSK, 1.3% over QC-Viterbi, and 0.2% over QCLDPC, indicating that the method maintains its effectiveness even as the redundancy in the transmitted data is reduced. This aspect is crucial for high-throughput systems where bandwidth efficiency is paramount.

The future scope of this research is ambitious, aiming to expand the operational capability to 128-bit operations. This scale-up is in direct response to the anticipated growth in the number of devices connecting to 5G networks, which will demand faster switching speeds and more robust error correction algorithms. The intention to improve upon the current research will likely focus on further optimizing the switching speed and reliability, ensuring that the 5G LTE network can keep pace with the rapid expansion of connected devices and the data-heavy demands of modern communication systems. This forward-looking approach highlights the ongoing need for innovation in 5G technology to support the burgeoning network of smart devices, industrial automation, and other emerging technologies that will define the digital landscape of the future.

Data Availability

The data used to support the research findings are available from the corresponding author upon request.

Acknowledgements

The authors would like to thank SJB Institute of Technology, JSS Academy of Technical Education, Bengaluru, JSS Science and Technology, Mysore, KS Institute of Technology, Bengaluru, Visvesvaraya Technological University (VTU), Belagavi and Vision Group on Science and Technology (VGST) Karnataka Fund for Infrastructure strengthening in Science & Technology Level – 2 sponsored “Establishment of Renewable Smart Grid Laboratory” for all the support and encouragement provided by them to take up this research work and publish this paper.

Conflicts of Interest

The authors declare no conflict of interest.

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